UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,325	12/29/2003	Colin Whitby-Strevens	APPL-P3015	1716

65201 7590 08/09/2007
GAZDZINSKI & ASSOCIATES, P.C.
11440 WEST BERNARDO COURT
SUITE 375
SAN DIEGO, CA 92127

EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
08/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,325	WHITBY-STREVENS ET AL.	
	Examiner	**Art Unit**	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _11 May 2007_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-39_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _29,38 and 39_ is/are allowed.

6)☒ Claim(s) _1-11,13-24 and 30-37_ is/are rejected.

7)☒ Claim(s) _12_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 39 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. (U.S. Pub. 2002/0152346) in view of Crutchfield et al. and what is well known in this art as evidenced by

Regarding claim 1, Stone et al. teach a method of transmitting data across a high-speed serial bus, the method comprising:

Generating a symbol (interpreted as data transfer) on an IEEE 1394-compliant PHY (Figure 5, item 120) having a port interface (Figure 3, items 88, 90);

Placing the symbol on the port interface (paragraphs 27, 38);

Placing the symbol in a FIFO (Figure 5, 136, 138, 140, 126, 128);

Removing the symbol from the FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 126, to 132, as indicated by the arrows, the symbol would have to be removed from the FIFO);

Sending the 8-bit byte to an IEEE 802.3-compliant PHY (paragraph 42; Figure 5, item 122; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

Stone et al. fails to explicitly teach the steps of loading and unloading data from the FIFOs in accordance with a first TX symbol clock and a second TX clock. Examiner notes that the IEEE 802.3 and IEEE 1394 busses transfer data at different rates, and thus require the data to be transferred into and removed from the FIFOs (Figure 5, 136, 138, 140, 126, 128) at different clock rates. Thus this limitation is inherently present in the system of Stone et al.

Stone et al. fail to teach generating a 10-bit symbol, scrambling the 10-bit symbol, encoding the 10-bit symbol, and deriving an 8-bit byte from the removed 10-bit symbol.

Crutchfield et al. teach sending a 10-bit signal on an IEEE 1394 bus, scrambling the symbol, encoding it, and transmitting it on the bus to the destination where it is decoded into an 8-bit word for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Stone et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Regarding claim 2, Stone et al. and Crutchfield et al., fail to explicitly teach wherein a symbol is removed from the FIFO on four out of every five GMII TX clock cycles. Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to remove a symbol from the FIFO on every GMII TX clock cycle in order for processing to continue. Removing a symbol on every clock cycle would include removing a symbol on four out of every 5 GMII TX clock cycles, and therefore meets this limitation.

Regarding claim 3, Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to place a null symbol in the FIFO when no symbols were present to indicate that the FIFO were empty. This is evidenced by D'Ignazio et al. in column 4, lines 50 – 54.

Regarding claim 9, Stone et al. inherently teach sending the received 8-bit byte from the IEEE 802.3 compliant PHY to a device in accordance with a phase amplitude modulation clock, since Stone et al. teach an IEEE 802.3 interface.

* * *

Claims 4 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., and further in view of Thayer et al.

Regarding claim 4, Stone et al. teach a FIFO (Figure 5, 136, 138, 140, 126, 128) but fail to teach wherein the 8-bit byte is derived from the 10-bit symbol by using 8 bits from the extracted 10-bit symbol, and the two remaining bits are stored.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving an 8-bit byte from a 10-bit symbol, they do show, for example, how two 16-bit symbols may be derived from a single 24-bit symbol. Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other varying-bit symbol permutations.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Stone et al. and Crutchfield et al. for the purpose of improving performance.

Claims 5 – 8 follow similar methodology as claim 4 and are rejected using the same rationale as above.

* * *

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., Tatum et al., Thayer et al., and further in view of Anderson et al.

Regarding claim 10, Stone et al. teach a method of transmitting data across a high-speed serial bus, the method comprising:

Receiving an 8-bit byte (paragraph 42; Figure 5, item 122; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

Stone et al. fails to explicitly teach the steps of loading and unloading data from the FIFOs in accordance with a first clock and a second clock. Examiner notes that the IEEE 802.3 and IEEE 1394 busses transfer data at different rates, and thus require the data to be transferred into and removed from the FIFOs (Figure 5, 136, 138, 140, 126, 128) at different clock rates. Thus this limitation is inherently present in the system of Stone et al.

If the received 8-bit byte contains a null symbol, then deleting the null symbol (Examiner takes official notice that it is old, and well known in the art to remove data padding upon receiving a piece of data for processing. White et al. evidence this in column 2, lines 16 – 20, column 4, lines 1 – 4, and Figure 6.

Else, storing the 8-bit byte in a register (Examiner takes official notice that a FIFO may be implemented using registers, as evidenced by Kohn in column 7, lines 8 – 10)

Receiving a second 8-bit byte that does not contain a null symbol and storing the second 8-bit byte in a second register (Examiner takes official notice that a FIFO may be implemented using multiple registers, as evidenced by Kohn in column 7, lines 8 – 10);

Stone et al. teach a FIFO (Figure 5, 136, 138, 140, 126, 128) but fail to teach assembling a 10-bit symbol from the 8-bit byte stored in the first register and appending two bits from the 8-bit byte stored in the second register.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving assembling a 10-bit symbol from an 8-bit byte stored in a first register and 2 bits in a second register, they do show, for example, how two a 24-bit symbol can be assembled from 3 8-bit symbols (Figure 11D). Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other permutations of the same method.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Stone et al. and Crutchfield et al. for the purpose of improving performance.

Stone et al. teach placing the symbol in a FIFO, removing the 10-bit symbol from the first FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 126, to 132, as indicated by the arrows, the symbol

would have to be removed from the FIFO) and sending the decoded 10-bit symbol to an IEEE 1394 compliant PHY (Figure 5, item 120).

Stone et al. fail to teach flagged decoding on the assembled 10-bit symbol.

Crutchfield et al. teach receiving a 10-bit signal on an IEEE 1394 bus, and performing 8B10B and control decoding it for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Stone et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Stone et al. fail to teach the IEEE 802.3-compliant PHY having a GMII interface.

Tatum et al. teach using a GMII interface for the purpose of providing high speed data transfer with low cost of implementation and maintenance, in addition to being compatible with previous Ethernet standards (column 2, lines 6 – 26).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a GMII interface as taught by Tatum et al. into the apparatus of Stone et al. for purpose of providing high speed data transfer with low cost of implementation and maintenance, in addition to being compatible with previous Ethernet standards. This would have been obvious to improve the performance of the system.

Stone et al, Crutchfield et al., and Thayer et al. fail to teach placing the decoded 10-bit signal into a second FIFO in accordance with a third clock, removing the decoded 10-bit symbol from the second FIFO and sending the decoded 10-bit symbol to an IEEE 1394-compliant PHY.

Anderson et al. teach placing the symbol in a second FIFO (Figure 1, item 5);

In accordance with a third clock (column 7, lines 64 – 66):

Removing the decoded symbol from the second FIFO (column 9, lines 13 – 15);

Sending the decoded symbol to an IEEE 1394-compliant PHY (Figure 1, item 2).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the method of Anderson et al. into the method of Stone et al, Crutchfield et al., and Thayer et al. for the purpose of maximizing the opportunity to successfully transmit useful information within an allocated time (column 6, lines 38 – 41. This would have been obvious in order to improve the performance of the system.

* * *

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., in view of Thayer et al., in view of Anderson et al., and further in view of Voit.

Regarding claim 11, Stone et al., Crutchfield et al., Thayer et al., and Anderson et al. fail to teach wherein the second clock is phase locked to the third clock.

Voit teaches phase locking different clock signals together in order to reduce setup and hold times associated with the components (column 5, lines 45 – 65).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to phase lock, as taught by Voit, the second and third clocks of Stone et al., Crutchfield et al., Thayer et al., and Anderson et al., for the purpose of reducing setup and hold times within the system, thereby improving system performance.

* * *

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al.

Regarding claim 13, Stone et al. teach a method of transmitting data across a high-speed serial bus, the method comprising:

Generating a symbol (interpreted as data transfer) on an IEEE 1394-compliant PHY (Figure 5, item 120) having a port interface (Figure 3, items 88, 90);

Placing the symbol on the port interface (paragraphs 27, 38);

Placing the symbol in a FIFO (Figure 5, 136, 138, 140, 126);

Removing the symbol from the FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 126, to 132, as indicated by the arrows, the symbol would have to be removed from the FIFO);

Sending the 8-bit byte to an IEEE 802.3-compliant PHY (paragraph 42; Figure 5, item 122; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

Stone et al. fails to explicitly teach the steps of loading and unloading data from the FIFOs in accordance with a first clock and a second clock. Examiner notes that the IEEE 802.3 and IEEE 1394 busses transfer data at different rates, and thus require the data to be transferred into and removed from the FIFOs (Figure 5, 136, 138, 140, 126, 128) at different clock rates. Thus this limitation is inherently present in the system of Stone et al.

Stone et al. fail to teach generating a 10-bit symbol, flagged encoding the 10-bit symbol, and deriving an 8-bit byte from the removed 10-bit symbol.

Crutchfield et al. teach sending a 10-bit signal on an IEEE 1394 bus, flagged encoding the symbol, and transmitting it on the bus to the destination where it is decoded into an 8-bit word for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Stone et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Regarding claim 14, Stone et al. and Crutchfield et al., fail to explicitly teach wherein a symbol is removed from the FIFO on four out of every five GMII TX clock cycles. Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to remove a symbol from the FIFO on every GMII TX clock cycle in order for processing to continue. Removing a symbol on every clock cycle would include removing a symbol on four out of every 5 GMII TX clock cycles, and therefore meets this limitation.

Regarding claim 15, Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to place a null symbol in the FIFO when no symbols were present to indicate that the FIFO were empty. This is evidenced by D'Ignazio et al. in column 4, lines 50 – 54.

Regarding claim 21, Stone et al. inherently teach sending the received 8-bit byte from the IEEE 802.3 compliant PHY to a device in accordance with a phase amplitude modulation clock, since Stone et al. teach an IEEE 802.3 interface.

* * *

Claims 16 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., and further in view of Thayer et al.

Regarding claim 16, Stone et al. teach a FIFO (Figure 5, 136, 138, 140, 126) but fail to teach wherein the 8-bit byte is derived from the 10-bit symbol by using 8 bits from the extracted 10-bit symbol, and the two remaining bits are stored.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving an 8-bit byte from a 10-bit symbol, they do show, for example, how two 16-bit symbols may be derived from a single 24-bit symbol. Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other permutations of the same method.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Stone et al. and Crutchfield et al. for the purpose of improving performance.

Claims 17 – 20 follow similar methodology as claim 4 and are rejected using the same rationale as above.

* * *

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., and further in view of Thayer et al.

Regarding claim 22, Stone et al. teach a method of transmitting data across a high-speed serial bus, the method comprising:

Receiving an 8-bit byte on an IEEE 802.3-compliant PHY (Figure 5, item 122; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

Stone et al. fails to explicitly teach the steps of loading and unloading data from the FIFOs in accordance with a first clock and a second clock. Examiner notes that the IEEE 802.3 and IEEE 1394 busses transfer data at different rates, and thus require the data to be transferred into and removed from the FIFOs (Figure 5, 136, 138, 140, 126, 128) at different clock rates. Thus this limitation is inherently present in the system of Stone et al.

If the received 8-bit byte contains a null symbol, then deleting the null symbol (Examiner takes official notice that it is old, and well known in the art to remove data padding upon receiving a piece of data for processing. White et al. evidence this in column 2, lines 16 – 20, column 4, lines 1 – 4, and Figure 6.

Storing the 8-bit byte in a register (Examiner takes official notice that a FIFO may be implemented using registers, as evidenced by Kohn in column 7, lines 8 – 10);

Receiving a second 8-bit byte that does not contain a null symbol and storing the second 8-bit byte in a second register (Examiner takes official notice that a FIFO may be implemented using multiple registers, as evidenced by Kohn in column 7, lines 8 – 10);

Stone et al. teach a FIFO (Figure 5, 136, 138, 140, 126) but fail to teach assembling a 10-bit symbol from the 8-bit byte stored in the first register and appending two bits from the 8-bit byte stored in the second register.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving assembling a 10-bit symbol from an 8-bit byte stored in a first register and 2 bits in a second register, they do show, for example, how two a 24-bit symbol can be assembled from 3 8-bit symbols (Figure 11D). Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other permutations of the same method.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Stone et al. and Crutchfield et al. for the purpose of improving performance.

Stone et al. teach placing the symbol in a FIFO (Figure 5, 136, 138, 140, 126), removing the 10-bit symbol from the first FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 126, to 132, as indicated by the arrows, the symbol would have to be removed from the FIFO) and sending the decoded 10-bit symbol to an IEEE 1394 compliant PHY (Figure 5, 120).

Stone et al. fail to teach flagged decoding on the assembled 10-bit symbol.

Crutchfield et al. teach receiving a 10-bit signal on an IEEE 1394 bus, and decoding it for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Stone et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Regarding claim 23, Stone et al. inherently teach wherein a received data valid state is asserted on the IEEE 802.3-compliant PHY since IEEE 802.3 inherently contains a receive data valid state as described in the IEEE 802.3 specification, page 17, section 22.2.2.6.

* * *

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., Thayer et al. and what is old and well known in this art as evidenced by Smith et al.

Regarding claim 24, Examiner takes official notice that it is old and well known in this art to use a FIFO for speed compensating between two busses of different speeds.

Smith et al. evidence this (column 2, lines 45 – 50 teach that speed compensating is done via a padding algorithm. Column 6, lines 23 –24 teach that Figure 6, item 204 is a padding unit. Column 6, lines 37 – 40 teach that Figure 6, item 204 contains a FIFO. Therefore, the FIFO is, at least in part, responsible for the data padding, which is responsible for speed compensation between the IEEE 802.3-compliant PHY and IEEE 1394-compliant PHY.).

* * *

New claims 30 – 36 are of a broader scope but of similar subject matter as claims 1, 10 and 11, and are rejected under similar rationale. Claim 37 is of a broader scope, but similar rationale as claims 9 and 21 and is rejected under the similar rationale.

Allowable Subject Matter

Claims 29, 38 and 39 are allowed.

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither teaches nor suggests all of the claimed subject matter of claim 12, including "**wherein frequency of null character deletion is used to control a phased locked loop, the phase locked loop associated with the second clock.**"

Response to Arguments

Applicant's arguments filed 5/11/2007 have been fully considered but they are not persuasive.

Regarding Applicant's argument that neither Stone nor Crutchfield suggest a FIFO, Examiner points to Fig 5, items 136, 138, 140, 126, 128 of Stone, which are described as queues. Examiner notes that a queue is the same as a FIFO, as evidenced by Wikipedia's definition of a FIFO (see attached reference).

Regarding Applicant's argument that Stone and Crutchfield fail to teach generating a 10-bit symbol on an IEEE 1394-compliant PHY and sending the 8-bit byte to an IEEE 802.3 compliant PHY, Examiner notes that Stone is relied upon for generating a symbol on an IEEE 1394-compliant PHY (interpreted as a physical layer of an IEEE 1394 interface) and sending the 8-bit byte to an IEEE 802.3 compliant PHY. Crutchfield is relied upon for showing why using a 10-bit transmission packets is beneficial to the performance and reliability of the bus. As stated in the office action, Examiner interprets the steps of generating a symbol as part of a data transfer, and the

IEEE 1394-compliant PHY does participate in data transfers (par. 42), and thus meets this limitation.

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner notes that Crutchfield is concerned with improving the performance of an IEEE-1394 bus (par. 12). Stone is concerned with using the IEEE-1394 bus (ABSTRACT). It is well established that the marketplace favors electronic systems that perform faster with greater reliability, and thus, obvious to one of ordinary skill in this art, at the time of invention by Applicant, to modify the system of Stone to use the scrambling/encoding/transmission means of Crutchfield for the purpose of improving the performance of the IEEE 1394 bus, and thus the performance of the entire device.

Regarding Applicant's argument that there is no motivation to combine the teachings of Thayer with Stone and Crutchfield, Examiner notes that KSR forecloses the argument that a specific teaching, suggestion, or motivation is required to support a finding of obviousness. See the recent Board decision *Ex parte Smith*, --USPQ2d--, slip op. at 20, (Bd. Pat. App. & Interf. June 25, 2007) (citing KSR, 82 USPQ2d at 1396) (available at http://www.uspto.gov/web/offices/dcom/bpai/prec/fd071925.pdf). Thayer is concerned with the transmission of data between devices that are connected via a bus, and improving system performance by data padding and alignment (col. 1, lines 10 – 17; col. 2, lines 10 – 18). Stone is also concerned with the transmission of data between devices that are connected via a bus (a bus is a form of a network; ABSTRACT), and Crutchfield is also concerned with the transmission of data between

devices that are connected via a bus (par. 11). Therefore, Examiner finds it would have been obvious to combine Stone with Crutchfield and Thayer for improving the performance of the system. This would have been obvious since it is well recognized that the marketplace favors systems with better performance.

Regarding Applicant's argument that there is no motivation to combine Anderson with Stone, Crutchfield, and Thayer, Examiner notes that Anderson is concerned with improving the performance of an IEEE 1394 bus, like Crutchfield, and teaches a means to do so through the use of a FIFO.

Examiner believes to have addressed the remainder of the arguments in the responses detailed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100